

10-02-02

2804



- 1 -

Cyntec-9001(09/867,644)

RECEIVED
TECHNOLOGY CENTER 2800
OCT - 14 2002
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

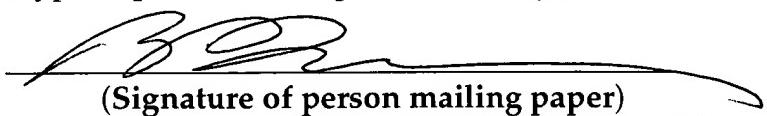
In re application of: Horng-Yih Juang, et al :Date: September 30, 2002
5 Serial No.: 09/867,644 :Group No.: 2826
Filed: May 29, 2001 :Examiner: A. Sefer
Attorney Docket No.: Cyntec-9001 :@(703)605-1227

5/a
F-JONES
10-8-02

CERTIFICATION UNDER 37 CFR 1.10

10 I hereby certify that this Office Response Transmittal and the documents referred to as enclosed therein are being deposited with the United States Postal Service on this date September 30, 2002 in an envelope as "Express Mail Post Office to Addressee" Mailing Label Number EU578845595US addressed to the: Commissioner of Patents and Trademarks, Washington, D. C. 20231.

15 Bo-In Lin
(Type or print name of person mailing papers)


(Signature of person mailing paper)

20 NOTE: Each paper or fee referred to as enclosed herein has the number of the "Express Mail" mailing label placed thereon to mailing. 37 CFR 1.10(b).

25 To the Commissioner of Patents and Trademarks:

AMENDMENT

30 Dear Sir:

In response to the Examiner's Action mailed on July 3, 2002, please amend the above noted Application as set forth below.

35

I. Please amend the specification as set forth below:

a) On Page 1 please amend the first paragraph of "Description of the Prior Art" as set forth below:

35

September 30, 2002

5

10

15

For those of ordinary skill in the art, the process of manufacturing a resistor with precisely controlled low resistance becomes a challenge for several reasons. As that shown in Fig. 1, a conventional resistor 100 is supported on a ceramic substrate 102 that includes a input electrode 104 and an output electrode 106 formed on two opposite ends on the ceramic substrate 102. A layer of thin resistive film 108 is formed on the top surface 112 of the ceramic substrate 102 between two electrodes 104 and 106 and a preservation protective layer 110 is formed on top of the resistive film 108. The resistor 100 with such a configuration can be mounted onto a printed circuit board with a surface mount technology (SMT) for establishing connection through the electrodes to the external circuits. Alternatively, the top surface 114 of the input electrode 104 and the top surface 116 of the output electrode 106 can be soldered to circuits on to printed circuit board by applying a reflow process.

II. Please amend claims 15 to 42 as set forth below: